Porous Si Nanowires from Cheap Metallurgical Silicon Stabilized by a Surface Oxide Layer for Lithium Ion Batteries

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In the quest to develop next generation lithium ion battery anode materials, satisfactory electrochemical performance and low material/fabrication cost are the most desirable features. In this article, porous Si nanowires are synthesized by a cost-effective metal-assisted chemical etching method using cheap metallurgical silicon as feedstock. More importantly, a thin oxide layer (≈3 nm) formed on the surface of porous Si nanowires stabilizes the cycling performance of lithium ion batteries. Such an oxide coating is able to constrain the huge volume expansion of the underlying Si, yet it is thin enough to ensure good permeability for both lithium ions and electrons. Therefore, the extraordinary storage capacity of Si can be well retained in prolonged electrochemical cycles. Specifically, Si/SiO_x nanowires deliver a reversible capacity of 1503 mAh g^{-1} at the 560th cycle at a current density of 600 mA g^{-1}, demonstrating an average of only 0.04% drop per cycle compared with its initial capacity. Furthermore, the highly porous structure and thin Si wall facilitate the electrolyte penetration and shorten the solid-state lithium transportation path, respectively. As a result, stable and satisfactory reversible capacities of 1297, 976, 761, 548, and 282 mAh g^{-1} are delivered at current densities of 1200, 2400, 3600, 4800, and 7200 mA g^{-1}, respectively.

1. Introduction

In pursuit of lithium ion batteries (LIBs) with high energy density, anode plays a crucial role in acting as an effective site for reversibly accommodation of lithium ions.[1] Various new anode materials with higher theoretical capacities have been proposed to replace the current state-of-the-art graphite anode.[2] Among all, silicon has attracted most attention with an outstanding theoretical capacity of 4200 mAh g^{-1} (forming $Li_{4.4}Si$ in full lithiation state), providing a tremendous increment compared with that of the current commercialized graphite anodes (372 mAh g^{-1}, Li_6C).[3,4] However, inevitable huge volume changes (as high as 311%) occur during charge and discharge processes of a silicon anode, leading to undesired cracking, loss of electric contact, and finally, fast fading of capacity.[5] Besides, the low lithium diffusivity of silicon also limits its electrochemical performance. Therefore, a major challenge in silicon anode research is to retain its high capacity during cycling process.

It has been widely recognized that, compared with their bulk counterpart, nanosized anode material can better accommodate the large strain generated by volume changes during cycling process.[6] In the case of silicon anodes, various nanomorphologies, such as nanoparticles,[5,7] nanotubes,[4] nanowires,[8] and nanocomposites[9] have been fabricated, demonstrating much improved cyclic stabilities. Among all, nanowire structure has drawn much attention, due to its unique morphological advantages, including better accommodation of volume expansion than its bulk counter part, facile axial charge transport owing to their 1D structure, and fast lithium diffusion in radial direction. Various techniques have been developed to fabricate silicon nanostructures, such as fluid–liquid–solid growth,[10] and chemical vapor deposition (CVD).[11,12] However, expensive raw materials or complex reaction environment are often required by these methods. Therefore, an urgent challenge is to develop silicon anodes using both cheap raw materials and a cost-effective technique, while being capable of retaining its high capacity during cycling process.

Metal-assisted chemical etching (MCE) is a simple and low-cost wet chemical technique for the fabrication of silicon nanostructures.[13] Moreover, various structural parameters, including cross section area, aspect ratio, and porosity level, can be controlled during the etching process.[14] Unique mesoporosity can be achieved by well controlled MCE, which is beneficial for electrolyte penetration and accommodation of volume expansion during lithium ion insertion and

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extraction processes.[15] Based on this method (i.e., MCE), Huang et al. fabricated silicon nanowire arrays using a p-type, (100) oriented silicon wafer as a substrate.[16] Qu et al. and To et al. both reported the synthesis of porous Si nanowires by performing MCE on highly doped n-type Si wafer.[17a,b] More recently, Ge et al. used boron-doped silicon wafer as the starting substrate and developed porous silicon anode with a stable capacity around 2000 mAh g^{-1} over 250 cycles, demonstrating excellent cyclic stability.[15] However, as mentioned, in most literature MCE of silicon requires expensive electronic grade silicon wafers as feedstock. In order to effectively reduce materials cost, by applying MCE method, Park and co-workers utilized cheap bulk Si particles to fabricate multidimensional Si, consisting of nanowire shell and microsized core.[18] Subsequently, the same group demonstrated the synthesis of 3D macroporous Si anode also by MCE method.[19] However, due to the existence of the microsized Si core, the reported electrochemical tests all terminated before 100 cycles. Another inexpensive silicon raw materials, such as metallurgical silicon, have been recently explored as the raw material for synthesis of mesoporous silicon nanowires by MCE. The existence of metal impurities is able to assist the formation of mesopores. However, the reversible capacity of such nanowires can only retain up to 50 cycles, indicating a huge room for improvement in terms of electrochemical cyclic stability of such low-cost silicon anodes.[20]

Herein, we report porous Si nanowires stabilized by a surface oxide layer (Si/SiO_x) fabricated by low-cost MCE technique, using cheap metallurgical silicon as feedstock. In such unique architecture, a thin layer of SiO_x coating (≈3 nm) was purposely introduced to the surface of porous Si nanowires by a facile post annealing process. Compared with pure Si, amorphous SiO_x ($x < 2$) layer has limited lithium storage capacity, but much smaller volume expansion coefficient during the lithium insertion and extraction processes, thus constraining the huge volume expansion of silicon and leading to a significant improvement in overall cyclic stability.[21,22]

2. Results and Discussion

The schematic representation of fabrication process of porous Si/SiO_x nanowires by MCE is shown in **Figure 1**. By immersing cheap silicon feedstock, metallurgical Si, in a solution of silver nitrate ($AgNO_3$) and hydrogen fluoride (HF), Ag nanoparticles were deposited at the metallurgical Si surface. Followed by an etching process involving strong acid (HF) and oxidant (H_2O_2), Ag nanoparticles penetrated into the silicon granule, resulting in the formation of Si nanowires.[23] Besides, the dissolution of metal impurities inside metallurgic Si also assisted in the pore formation process, resulting in porous Si nanowires.[20] Subsequently, in order to constrain the huge volume expansion of Si and thus enhance the cyclic stability of such an anode material, a thin layer of SiO_x was applied to the porous silicon nanowires surface by a post annealing process.

The morphology of Si/SiO_x nanowires was characterized using transmission electron microscopy (TEM). **Figure 2**a,b shows low magnification TEM images of Si/SiO_x nanowires, demonstrating successful formation of nanowire structure by MCE technique. Furthermore, the difference in contrast of these two low magnified TEM images indicates the existence of porous structure within these nanowires. Such observation is confirmed by closer examinations of Si/SiO_x nanowires in Figure 2c,d. The contours of Si/SiO_x nanowires are outlined in Figure 2c. As can be clearly observed in Figure 2c,d, mesopores evenly distribute throughout the entire nanowire structure. The dimension of each pore is measured and summarized in the bar shown in Figure S1 (Supporting Information). Based on TEM observation, the average pore size can be calculated to be around 14.1 nm. Such high porosity is desirable for electrolyte penetration during electrochemical tests, thus enlarging the electrode–electrolyte interface and facilitating the solid-state lithium diffusion. The dotted pattern of fast-Fourier transform (FFT) shown in the inset of Figure 2d indicates the single crystalline nature of Si, which is beneficial to the lithium ion diffusion within such an anode material. Figure 2e,f shows high resolution TEM images of Si/SiO_x nanowires. The crystalline nature of Si is further confirmed. As shown in the high resolution transmission electron microscopy (HRTEM) image (Figure 2f), the nanowires are well crystalline with clear lattice fringes with d-spacing of 3.1 Å, corresponding to the (111) crystal plane of Si. Besides, a thin amorphous layer of SiO_x can be clearly identified at the surface of crystalline silicon, which will assist the accommodation of Si during the charge/discharge process, as will be discussed below. It has been well understood that the increment in oxygen content of silicon would lower the lithium insertion capability and increase the resistivity.[21] Therefore, the thickness of such an oxide layer was carefully controlled to be around 3 nm to constrain the huge volume expansion of underlying Si, without compromising the capacity and conductivity of the overall structure too much. As-obtained Si/SiO_x was further investigated with the aid of scanning electron microscopy (SEM). As shown in Figure S2 (Supporting Information), the nanowire morphology and porous structure can be unambiguously observed in high and low magnification SEM images, respectively, confirming the successful formation of porous nanowire structure.

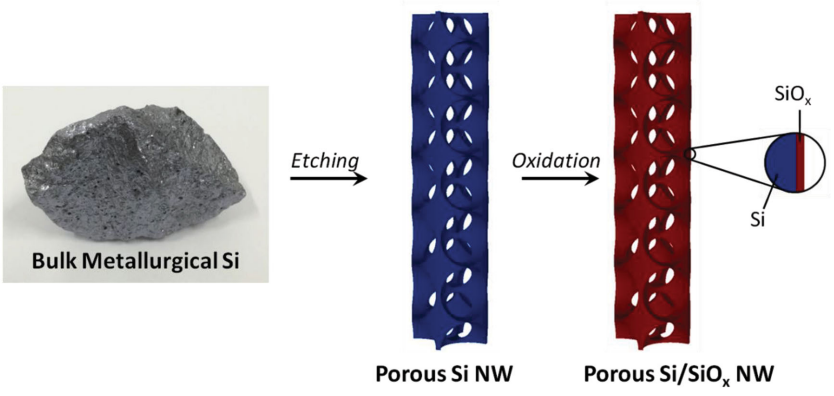

Figure 1. Schematic representation of the fabrication process of porous Si/SiO_x nanowires by MCE from metallurgical silicon.

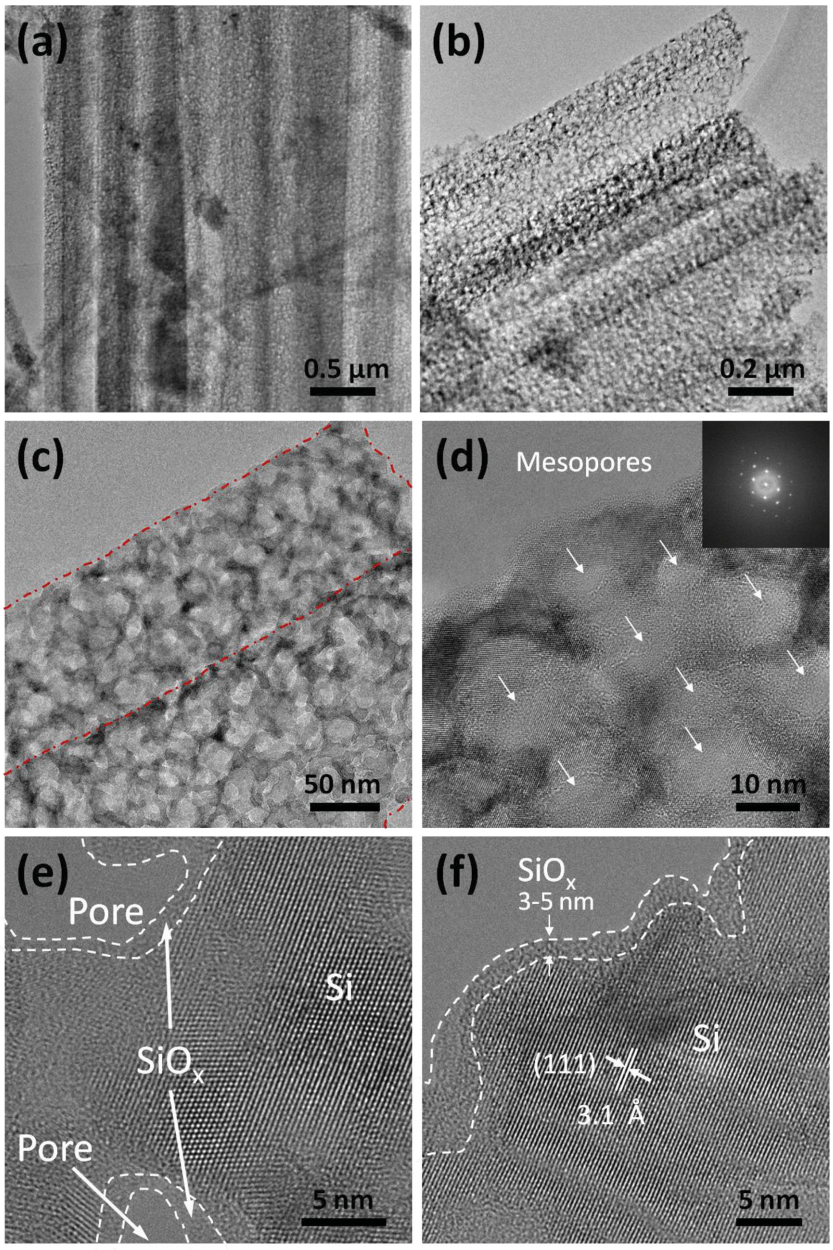

Figure 2. a–d) Low- and e,f) high-resolution TEM images of Si/SiO_x nanowires.

The porous structure of Si/SiO_x nanowires was characterized by the Brunauer–Emmett–Teller (BET) nitrogen sorption method. As shown in **Figure 3**a, Si/SiO_x nanowires show typical type I/IV adsorption/desorption isotherms, with hysteresis loops at both high and low pressures, indicating the existence of both micropores and mesopores. The microspores were originated from the void space between nanowires.[24] The formation of mesopores can be ascribed to the penetration of Ag nanoparticles and dissolved metal impurities inside metallurgical Si upon exposure to etchant solution.[14,20] The BET surface area of Si/SiO_x was calculated to be 135.3 $m^2\ g^{-1}$ with a total pore volume of 0.53 $cm^3\ g^{-1}$. Such a large surface area is favorable to enhance the lithium flux cross the electrolyte–electrode interface. The porous nature of Si/SiO_x nanowires was further characterized by the pore size distribution shown in Figure 3b. Calculated by the BET model from the adsorption branch of isotherms, the average pore size of Si/SiO_x nanowires is 14.0 nm, which is in good agreement to the observation from TEM images. Such a pore size is slightly smaller than that of porous pure Si nanowires.[20] The shrinkage in pore size can be attributed to the volumetric expansion of Si surface upon oxidation.

The surface oxide layer is assumed to be crucial for the cyclic stability during electrochemical tests. Therefore, secondary ion mass spectroscope (SIMS) analysis was used to study the oxygen content of Si/SiO_x nanowires in detail. In order to quantify the ratio between Si and O, a standard SiO_2 sample was used as the reference. **Figure 4**a shows the mass spectrum on porous Si/SiO_x nanowires (red) and SiO_2 (blue). The Si and O mass peaks on both Si/SiO_x (red) and SiO_2 (blue) are shown in Figure 4b,c, repectively. By referring to the atomic ratio of standard SiO_2, the x value of porous Si/SiO_x nanowires can be calculated to be 1.26 (Figure S3, Supporting Information), indicating the atomic percentage of Si and O are 44% and 46%, respectively. X-ray photoelectron spectroscopy (XPS) has also been performed on porous Si/SiO_x nanowires to further investigate the oxide layer. As shown in the survey spectrum of Si/SiO_x in Figure S4a (Supporting Information), the predominant O1s peak indicates the high oxidation degree of silicon. The Si 2p peak is shown in Figure S4b (Supporting Information), with energy positions attributed to different oxidation states indicated. As can be clearly observed, Si^{4+} and Si^0 are the prominent peaks with no obvious shoulder observed in-between, indicating the low percentage of sub-oxide states. Therefore, the oxide layer of Si/SiO_x is predominately SiO_2 by the postannealing process. Furthermore, the XPS elemental analysis shows that the surface atomic percentages of Si and O are around 45% and 55%, respectively. Such result is in good agreement with the atomic percentage obtained from SIMS measurement. The higher Si percentage compared with stoichiometric ratio of SiO_2 can be ascribed to the pure Si underlying the SiO_x surface. Therefore, based on the shallow signal detection depth of SIMS and XPS, the oxide layer is further confirmed to be very thin, which is consistent with the observation of TEM.

The electrochemical performance of Si/SiO_x nanowires as LIB anodes was examined in a coin cell with a lithium metal as counter electrode. **Figure 5**a shows the 1st and 2nd cycles of the cyclic voltammetry (CV) obtained at a scan rate of 100 $\mu V\ s^{-1}$ within a potential range of 0.01–1.5 V. A weak and

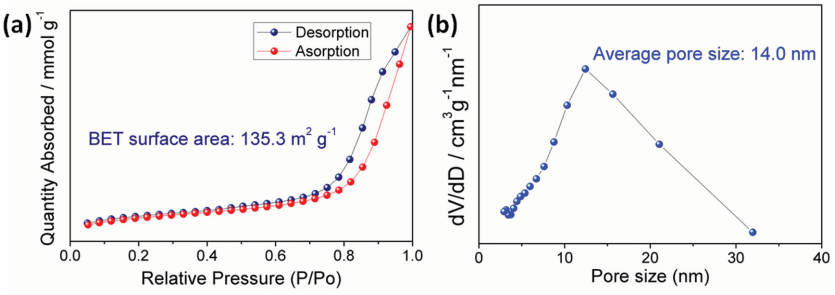

Figure 3. a) Nitrogen sorption isotherms and b) pore size distribution of Si/SiO_x nanowires by MCE.

broad cathodic peak centered around 0.8 V can be observed in the first cycle, corresponding to the formation of solid electrolyte interphase (SEI). This irreversible capacity loss is mainly related to the formation of the SEI layer as well as the electrochemical reaction of Li ions with SiO_2 oxide layer, which lead to the formation of either Li_2O, Si, and Li_4SiO_4 (irreversible products), or $Li_2Si_2O_5$ and Si (reversible products). This peak disappeared in the second cathodic scan. The main peak ranging from 0.015 to 0.27 V in the first cathodic scan can be ascribed to the formation of amorphous Li_xSi phase.[9] The peak reduces in amplitude in the second cycle, indicating the partially irreversible nature of this reaction. In the second cathodic scan, a new peak appeared at 0.14 V, corresponding to the reversible lithiation of amorphous Si domains.[25] Two peaks centered around 0.36 and 0.5 V are observed in both first and second anodic scans, corresponding to the delithiation process of amorphous Li_xSi to amorphous Si.[7]

The cyclic performance of porous Si/SiO_x and corresponding coulombic efficiencies at a current density of 800 mA g^{-1} are shown in Figure 5b. The initial discharge and charge capacities are 4513 and 1880 mAh g^{-1}, respectively, demonstrating an initial coulombic efficiency of 42%. Silicon oxide based anodes generally have a relatively low first cycle coulombic efficiency, generally ranging from 40% to 60%.[21,26] The unsatisfactory initial coulombic efficiency can be mainly attributed to the oxide surface of Si/SiO_x.[26,27] For pristine Si without any oxide surface layer, electrolyte reacts with its surface Si–H bonds to form organo-fluorine compound. In the case of Si/SiO_x, the underlying Si is protected and the oxide surface layer react with electrolyte in a similar manner as most metal oxides, where large amount of lithium ions participate in the irreversible reaction with lithium.[28] Therefore, a low initial coulombic efficiency can be expected. Besides, the large surface area of the porous Si/SiO_x nanowires also contributed to the low initial coulombic efficiency. Owing to the existence of meospores, the specific surface area of Si/SiO_x nanowires is higher that normal Si electrode mainly consisting of macropores. Therefore, SEI layer of larger area is formed in the first cycle, resulting in a relatively low first coulombic efficiency. The coulombic efficiency rose above 93% at the second cycle and kept close to 100% from the fifth cycle onwards. As shown

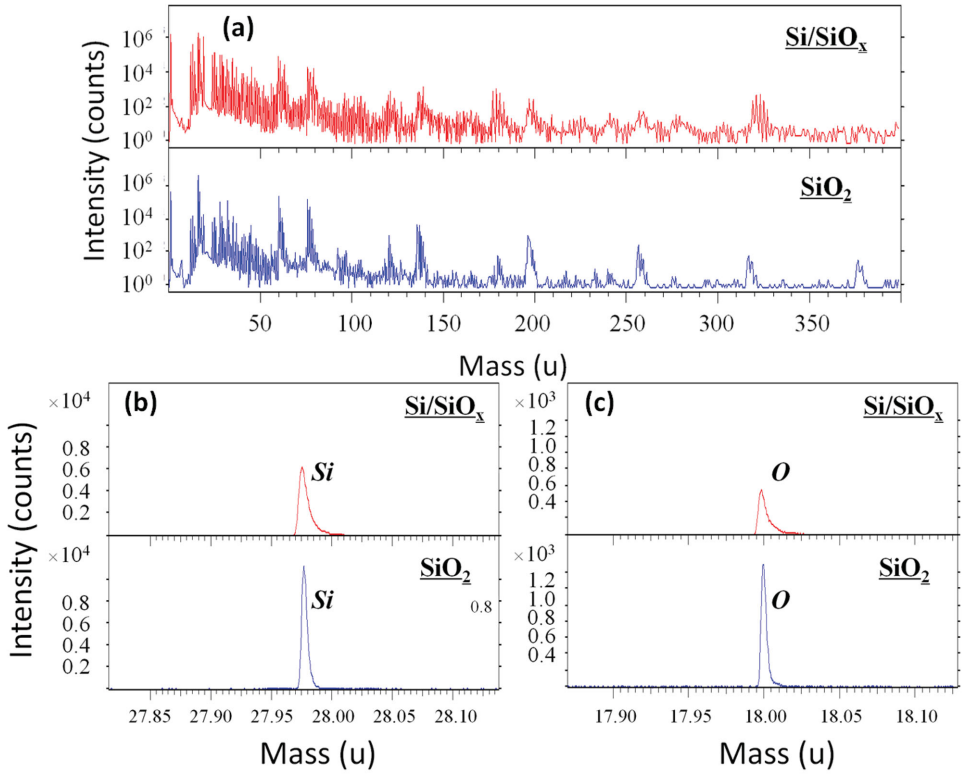

Figure 4. a) SIMS mass spectrum on porous Si/SiO_x (red) and SiO_2 (blue). b) Si and c) O mass peaks on Si/SiO_x (red) and SiO_2 (blue).

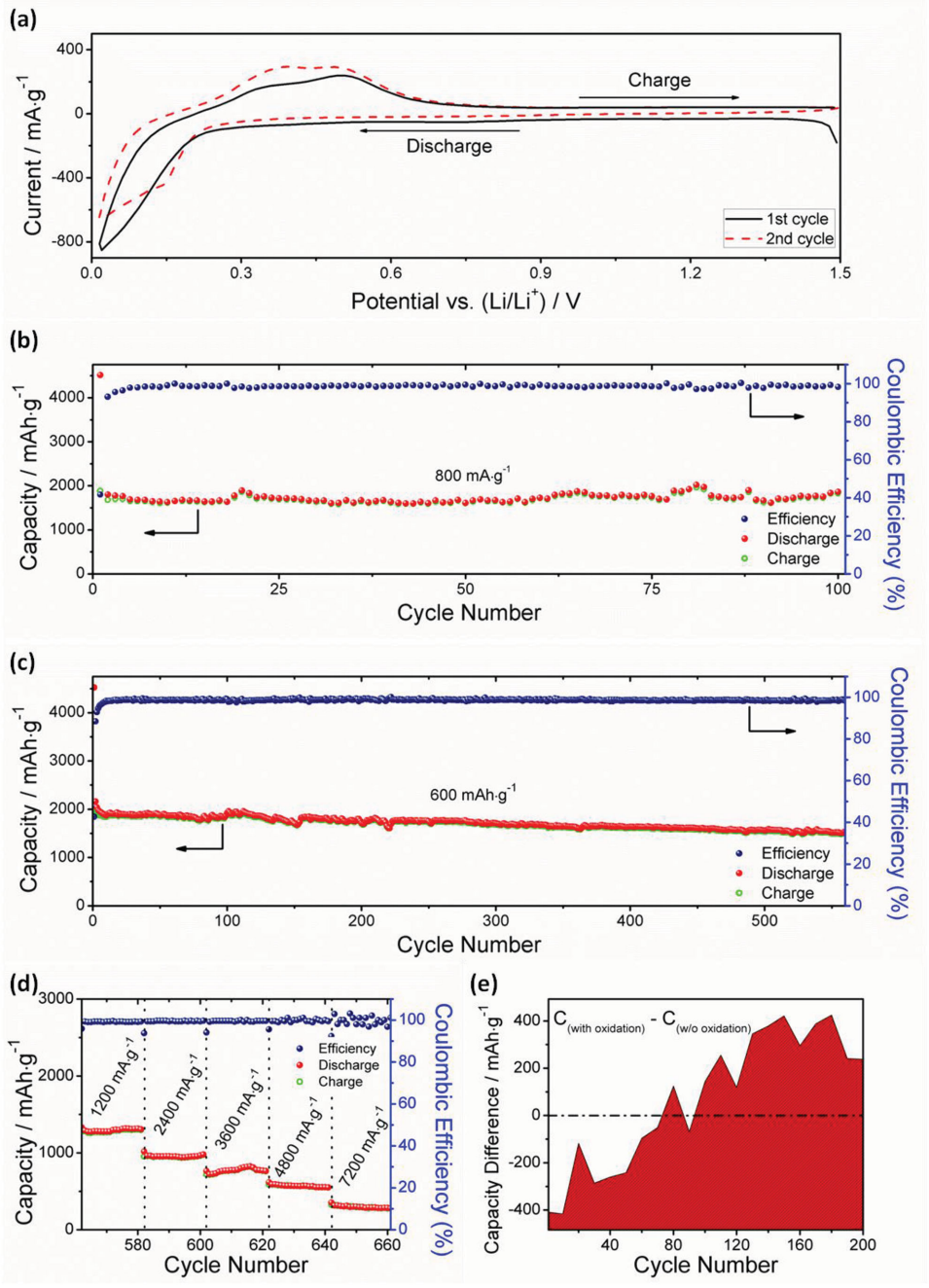

Figure 5. a) Cyclic voltammetry profiles of the first two cycles of Si/SiO_x nanowires. b) Cyclic performance of Si/SiO_x nanowires at a current density of 800 mA g^{-1}. c) Stability test at a current density of 600 mA g^{-1} and d) subsequent rate capability test at various current densities. e) Capacity difference between Si/SiO_x and Si nanowires at different stages of a cyclic test at a current density of 800 mA g^{-1}.

in Figure 5b, the anode consisting of Si/SiO_x demonstrated stable cyclic performance over the test range with a reversible capacity of 1802 mAh g^{-1} at 100th cycle.

In the literature, due to their huge volume expansion during charge/discharge processes, most Si-based anode were only able to be cycled up to 50 to 150 cycles.[10,11,29] To further examine the outstanding cyclic stability of such oxide coated porous Si nanowires, a fresh half cell using porous Si/SiO_x nanowires as active anode materials was electrochemically tested at a current density of 600 mA g^{-1} for 560 cycles. As shown in Figure 5c, the first reversible capacity is 1933 mAh g^{-1}, with an initial coulombic efficiency of 43%, which is comparable with that of the previous test at 800 mA g^{-1} and other Si-based anode materials reported in the literature. The restricted coulombic efficiency is attributed to the formation of SEI in the first cycle and the irreversible reaction between lithium and oxide coating: $SiO_x + Li = Si + x\ Li_2O$.[30] Based on the active material loading amount and electrode area, the first areal capacity of the proposed

electrode at current density of 0.8 mA cm^{-2} can be calculated to 2.56 mAh cm^{-2}. Such value is much higher than the areal capacity of metal oxide electrode materials,[31] and is better that of another reported Si-based electrode under similar current density.[32] The anode consisting of porous Si/SiO_x nanowires is able to deliver stable reversible capacity over the entire test range of 560 cycles. Specifically, the last charge capacity of Si/SiO_x is 1503 mAh g^{-1}, demonstrating an average drop of only 0.04% per cycle compared with its initial capacity. Such a long testing period for Si-based anode is not often found in literature where most works terminate cycling tests within 100 cycles.[4,7,10,33] The superior cyclic performance is mainly attributed to the following reasons: (1) surface oxidation layer of Si/SiO_x nanowires greatly buffers the volume changes of underlying Si and thus alleviating the pulverization problem; (2) evenly distributed mesopores further accommodate the volume expansion of Si and also facilitate the penetration of electrolyte; (3) thin Si walls also help to buffer the volume changes and shorten the lithium diffusion path length. After extended cyclings the SEI layer becomes very thick and physically blocks the migration of Li ions through the SEI layer. On the other hand the surface SEI layer might be damaged by the evaporation of the electrolytes at high temperatures. Therefore the unstable cycling performance is significant at higher current rates. In this sense the oxide protective layer is important. It is reasonable to assume that the SEI layer is relatively stable at low current (0.1 A). While at higher current (0.5 A) the internal temperature rises quickly and the decomposition/regeneration of the SEI is quicker. This process will physically block the migration of Li ions after certain times of cycling. The voltage profile of porous Si/SiO_x nanowires of 1st, 2nd, 10th, and 50th cycles at current density of 600 mA g^{-1} is in Figure S5 (Supporting Information). The large sloping plateau locates around 0.8 V in the first discharge profile disappears in subsequent cycles, corresponding to SEI formation process. The long plateau below 0.25 V can be attributed to the formation of Li–Si alloys. Upon cycling, Si is responsible for most of the reversible capacity, as the lithium insertion mainly occurs below 0.25 V from the second cycle. All charge profiles coincide well with each other, indicating the excellent cyclic behavior of porous Si/SiO_x nanowires.

The same cell after being cycle at a current density of 600 mA g^{-1} for 560 cycles was further tested for rate capability. As shown in Figure 5d, Si/SiO_x anode delivers reversible capacities of 1297, 976, 761, 548, and 282 mAh g^{-1} at the 20th cycle under current densities of 1200, 2400, 3600, 4800, and 7200 mA g^{-1}, respectively. Furthermore, no obvious capacity drop can be observed under each current density, demonstrating excellent rate performance. Such satisfactory high rate performance is mainly ascribed to the interconnecting mesopores to facilitate the electrolyte penetration and thin Si wall to shorten the lithium diffusion path. Electrochemical impedance spectroscopy (EIS) tests have been performed on coin cells fabricated from porous Si/SiO_x nanowires before and after 660 electrochemical cycles at various current densities up to 7200 mA g^{-1}. As shown in Figure S6 (Supporting Information), the shapes of two Nyquist plots are similar, each being composed of a semicircle and a quasi-straight line. It can be clearly observed that the cycled cell possesses smaller semicircle, indicating improved lithium ion diffusion through cycling process.

To further demonstrate the crucial effect of the surface oxide layer on the cyclic stability of porous Si nanowires, the capacity difference between Si/SiO_x and Si nanowires at a current density of 800 mA g^{-1} over 200 cycles is shown in Figure 5e. In the first cycle, the reversible capacity of Si/SiO_x is about 400 mA g^{-1} lower than that of pure Si nanowires. The difference is due to the limited lithium storage capability of SiO_x compared with that of Si. However, as indicated by the steep slope of the curve, the capacity difference reduces quickly as the cycling tests proceed. At cycle number 96, these two types of nanowires deliver almost the same reversible capacities. Beyond this point, Si/SiO_x nanowires are able to deliver higher capacity than that of Si nanowires. Specifically, at the 200th cycle, the reversible capacity of Si/SiO_x nanowires are 237 mA g^{-1} higher than that of Si nanowires, confirming the crucial effect of a surface oxide layer on accommodating the huge volume expansion of underlying Si and thus enhancing the cyclic stability of porous Si nanowires. The cycling performance of porous pristine Si nanowires is shown in Figure S7 (Supporting Information) for reference.

In order to investigate the effect of oxide thickness on electrochemical performance, porous Si/SiO_x nanowires with a relatively thick oxide layer were also fabricated by extending the annealing duration. As shown in the HRTEM image shown in Figure S8a (Supporting Information), oxide layer with thickness around 7 nm (Si/SiO_x-thick) was successfully applied to the crystalline Si surface. The corresponding electrochemical performance at current density of 800 mA g^{-1} is shown in Figure S8b (Supporting Information). The first discharge and charge capacities are 4903 and 1002 mAh g^{-1}, respectively, corresponding to a low initial coulombic efficiency of 20.4%. During the test period of 50 cycles, the reversible capacity of Si/SiO_x-thick gradually decayed to 750 mAh g^{-1}. By comparing the electrochemical cycling performances of porous Si nanowires coated with oxide of different thickness (0, ≈3, ≈7 nm), several conclusions can be drawn. First, surface oxide coating can effectively enhance the cyclic stability of Si nanowires. As discussed above, the oxide surface reacts with lithium to form Li_2O, silicates, and Li_xSi during electrochemical reaction. In nanoscale, the mechanical strength of material is governed by the strength of atomic bonds. Due to their higher ionicities, Li–O and Si–O bonds in lithiated SiO_x are stronger than Li–Si bonds in lithiated Si.[26] Therefore, the much stronger oxide coating on the surface of Si nanostructure is able to apply a constraining force on underlying Si. Such constraining effect is able to limit the volume expansion of Si core during electrochemical cycling. As known, the pulverization problem of Si-based electrode induced by its volume changes leads to fracture of Si structure and fast fading of capacity. Therefore, by constraining the volume expansion of underlying Si, the surface oxide layer is able to mitigate the fracture and pulverization problem, and thus enhancing the cyclic stability of composite structure.[34] Second, the specific capacity of Si nanowires is reduced by the oxide coating, and the thicker the oxide coating the lower the capacity. The strong oxide shell applies constraining force on Si core, thus limiting the extent of lithiation during cycling.[26] Besides, the existence of oxygen also reduces the overall capacity. Third, the initial coulombic efficiency is lowered by surface oxide coating. As described in previous section, thicker oxide requires more lithium ions to participate in the irreversible reaction between

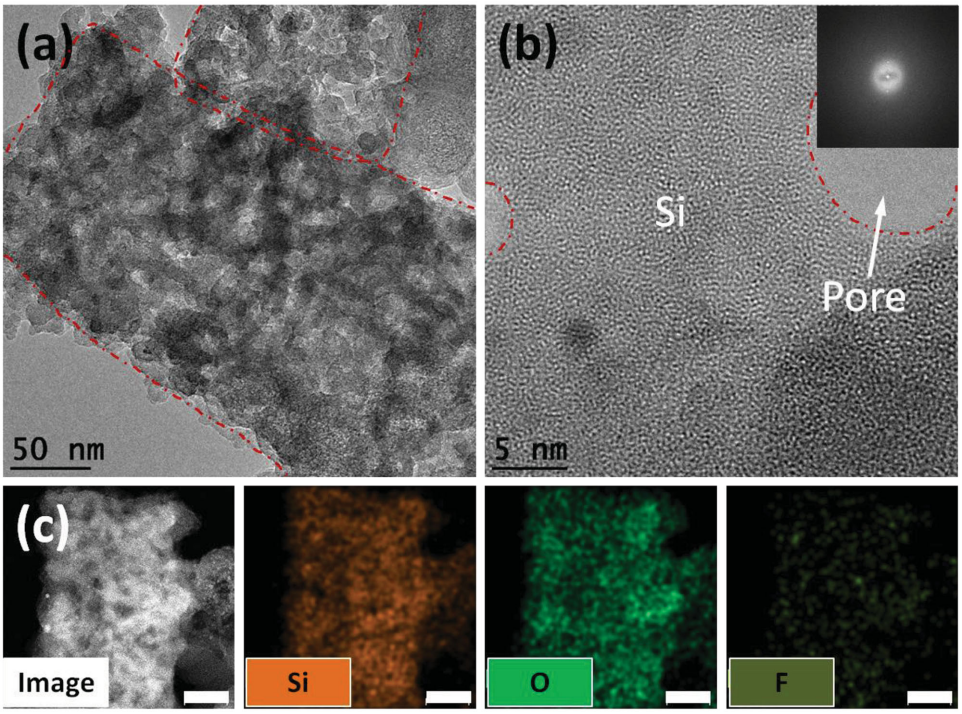

Figure 6. a) TEM and b) HRTEM images, and c) EDX mapping of Si/SiO_x nanowires after a cycling test (scale: 50 nm).

lithium and oxide, thus reducing the initial coulombic efficiency. Such phenomenon is also observed in most of other oxide anode materials.[35]

Cui and co-workers performed a detailed study on the thickness of surface oxide and Si walls on the electrochemical performance of oxide coated Si nanowires.[26] They found that oxide surface can significantly suppress the volume expansion of Si nanowires with diameter less than 50 nm. Cho and co-workers developed a core@shell bulk@nanowire Si anode and discussed the effect of SiO_2 coating thickness on its electrochemical performance.[27] They found bulk@nanowire Si anode with 7 nm oxide surface delivered the best overall electrochemical performance. These two works have demonstrated the crucial effect of oxide coating in the enhancement of overall cyclic stability. In the current work, in addition to oxide coating layer, we also incorporated mesoporous structure into the Si nanowires. As mentioned by many other works, such porous structure is beneficial to the penetration of electrolyte, accommodation of volume changes, and therefore the resultant electrochemical performance. Such improvement can be clearly demonstrated by the difference between electrochemical results. In the work by Cui and co-workers, all cycling performances terminated at the 10th cycle. The cycling tests done by Cho and co-workers stopped at 130th cycle. In contrast, by the incorporation of mesopores, porous Si/SiO_x nanowires reported in the current work delivered stable reversible capacities over a much longer range of 560 cycles at a current density of 600 mA g^{-1}.

The incorporation of porous structure and utilization of nanoscale electrode materials create lots of interparticle space and therefore reduce the resultant tap density in the final electrode. However, even calculated based on the volume of full lithiated stage, the volumetric capacity of Si is around 2200 Ah L^{-1}, which is about triple of that of graphite and higher than those of most of other alloying anode materials.[36] Therefore, even large void space is incorporated (over 200% void space compared with its initial volume), the capacity of Si anode and the final energy density for a full LIB cell are still much better than those of graphite and most other newly proposed anode materials in a full LIB cell where the volume for anode material is predetermined.

The morphology of porous Si/SiO_x nanowires after the cycling test was examined using TEM and is shown in **Figure 6**a,b. After being tested under harsh conditions, including extended cycling (over 600 electrochemical cycles) and at high current densities (up to 7200 mA g^{-1}), Si/SiO_x nanowires still preserve wire-like structure and no large difference can be observed compared with their morphology prior to electrochemical tests (Figure 2C). In addition, the clear difference in contrast in Figure 6a reveals the retention of mesopores. The shrinkage in pore diameter can be attributed to the SEI formation on the surface of nanowires. Under examination of high resolution TEM, Si becomes amorphous after electrochemical tests. This observation is confirmed by the selected area electron diffraction (SAED) pattern (inset of Figure 6b). Si/SiO_x nanowires were also examined by EDX mapping. As shown in Figure 6c, two major elements, namely, Si and O, can still be observed with similar intensities. As a result of electrolyte degradation and SEI formation, evenly distributed F can be also detected. The morphologies of Si/SiO_x electrode before and after cycling process are examined by SEM. As shown in Figure S9a,b (Supporting Information), the electrode surface became covered by SEI layer through cycling process. More importantly, as shown in the cross-section views (Figure S9c,d, Supporting Information), the thickness of the electrode only

increased form 43.6 to 50.4 μm after electrochemical test, corresponding to a slight increment of 16%. Such observation confirms the constraining effect of oxide layer on the volume expansion of Si-based electrode material.

3. Conclusion

In summary, a sustainable route from cheap metallurgical silicon to porous Si/SiO_x nanowires was successfully demonstrated for high-performance lithium ion batteries. With a surface oxide layer of suitable thickness, lithium ions can easily penetrate and react reversibly with underlying Si. More importantly, the huge volume expansion of Si during charge/discharge processes can be greatly accommodated by the surface oxide layer, resulting in a superior cycling performance. Specifically, a reversible capacity of 1503 mAh g^{-1} was delivered at the 560th cycle at a current density of 600 mA g^{-1}, demonstrating an average drop of only 0.04% per cycle compared with its initial capacity. Considering the inexpensive synthesis method (i.e., MCE) and cheap starting materials (i.e., metallurgical silicon), porous Si/SiO_x nanowires have great potential in the commercial application of next generation LIB.

4. Experimental Section

Si/SiO_x Nanowire Fabrication and Characterization: The surface of metallurgical silicon was first degreased in acetone and isopropanol, rinsed with Milli-Q deionized (DI) water, and then cleaned in a piranha solution (3:1 concentrated H_2SO_4/30% H_2O_2) for 15 min at 80 °C followed by rinsing by DI water. The Si nanowires were prepared by chemical etching of the surface of metallurgical silicon in $HF/AgNO_3$ (5.25/0.02 M) solution at room temperature and then in 10 M HF and 0.5 M H_2O_2. After etching, the Si samples were rinsed with DI water and dried by N_2. Si nanowire powder was obtained by direct scratching. Si/SiO_x nanowires were synthesized by heating at 500 °C in a control O_2 concentration in the CVD furnace. The morphology was observed with field emission scanning electron microscopy (FESEM, SU8010, Japan), and field emission transmission electron microscopy (FETEM, FEI Tecnai G2 F20 S-TWIN TMP, Hongkong). Surface elemental analysis was performed on a SIMS (TOF.SIMS 5, ION-TOF GmbH, Germany) and an XPS (Kratos Axis Ultra Dld, Japan).

Electrochemical Characterization: Electrochemical measurements were performed using two-electrode coin cells assembled in an argon filled glove box. For preparing the working electrodes, For the electrochemical investigation, 80 wt% Si/SiO_x active material nanowires, 15 wt% conductive carbon black, and 5 wt% poly(vinylidene fluoride) binder were mixed in *N*-methyl-2-pyrrolidone to form a slurry which was applied onto an etched aluminum foil current collector using doctor-blade technique and then dried at 100 °C for 12 h. Electrochemical measurements were carried out using 2032 type coin cells assembled in a glove box filled with Ar gas. Lithium foil (Foote mineral Co.) and 1 M $LiPF_6$ solution in a 1:1 ethylene carbonate and dimethyl carbonate were used as negative electrode and electrolyte, respectively. The electrolyte was supported by polypropylene based foil separator (PP Celgard Inc.). Galvanostatic charge/discharge tests were performed between 0.01 and 1.5 V at a scanning rate of 0.1 mV s^{-1} via a Zahner electrochemical workstation (IM6ex).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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